WHAT IS CLAIMED IS:

1. A method of forming a metal line in a semiconductor device, comprising the steps of:

(a) sequentially forming a first interlayer insulation film, an etch-stopping layer, and a second interlayer insulation film on a semiconductor substrate having a predetermined semiconductor structural layer;

(b) forming a contact hole which partially exposes the semiconductor structural layer by performing an etching process using an etching mask for the contact hole;

(c) forming a metal plug to bury the contact hole;

(d) sequentially forming an anti-diffusion film and a third interlayer insulation film on the whole structure;

(e) performing an etching process using an etching mask for a trench to form the trench in such a way that the second interlayer insulation film is over-etched by using the etch-stopping layer as an etching barrier; and

(f) forming a metal line to bury the trench.

2. The method of claim 1, wherein the etch-stopping layer is composed of SiC, SiN, or SiON.

3. The method of claim 1, wherein the first interlayer insulation film and the second interlayer insulation film are formed by depositing BPSG, PSG, USG, or FSG, or by a film in which fluorine, hydrogen, boron, or phosphorous is locally diffused into SiO or SiO_2 in a substitutional or interstitial manner.

4. The method of claim 1, wherein the etching process in the step (b) is performed by using a $C_xH_yF_z$ gas (x, y, and z are 0 or any natural number) as a main etchant gas and an inert gaseous atom or a molecule of O_2, N_2, SF_6, Ar, or He as an additive gas.